Docket No.: PEK-IN1137

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : JOSEF FAZEKAS ET AL.

Filed : CONCURRENTLY HEREWITH

Title : ELECTROMIGRATION TEST STRUCTURE FOR DETECTING THE RELIABILITY OF WIRING

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

S i r :

In accordance with 37 C.F.R. 1.98 copies of the following patents and/or publications are submitted herewith:

U.S. Patent No. 5,777,486 (Hsu), dated July 7, 1998;

Patent Abstracts of Japan 06077299 (Hiroshi), dated March 18, 1994;

Patent Abstracts of Japan 2000003947 (Shinji), dated January 7, 2000;

Patent Abstracts of Japan 2000174085 (Yumi), dated June 23, 2000;

European Patent Application EP 0 448 273 A1 (Chesire et al.), dated September 25, 1991;

Schafft, H. A.: "Reliability Test Chips: NIST 33 & NIST 34 for JEDEC Inter-Laboratory Experiments and More", 97 IRW Final Report, pp. 144 and 145;

Sriram, T. S.: "Electromigration Test Structure Designed to Identify via Failure Modes", IEEE, 2000, pp. 155-157;

International Search Report, dated February 21, 2003.

Respectfully submitted,

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Date: August 25, 2003

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FORM PTO-1449 (SUBSTITUTE) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT (37 CFR 1.98(b))	Attorney Docket No.: PEK-In1137 Appl. No.: Applicant: JOSEF FAZEKAS ET AL. Filing Date: August 25, 2003 Group Art Unit:

EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
	A	5,777,486	7/7/98	Hsu			
	B						
	C						
	D						
	E						
	F						
	G						
	H						
	I						

FOREIGN PATENT DOCUMENT

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSL. YES	TRANSL. NO
	J	06077299	3/18/94	Japan				
	K	2000003947	1/7/00	Japan				
	L	2000174085	6/23/00	Japan				
	M	0 448 273 A1	9/25/91	Europe				
	N							

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

		Schafft, H. A.: "Reliability Test Chips: NIST 33 & NIST 34 for JEDEC Inter-Laboratory Experiments and More", 97 IRW Final Report, pp. 144 and 145
		Sriram, T. S.: "Electromigration Test Structure Designed to Identify via Failure Modes", IEEE, 2000, pp. 155-157

EXAMINER	DATE CONSIDERED